Chettinad College of Engineering & Technology
Approved by AICTE, New Delhi and Affiliated to Anna University, Chennai.

Department of Electronics and Communication Engineering

EC8453-Linear Integrated Circuits

Unit III - MCQ Bank

1. A Determine output voltage of analog multiplier provided with two input signal V_x and V_y.

A) $V_o = (V_x \times V_x) / V_y$

B) $V_o = (V_x \times V_y / V_{ref}$

C) $V_o = (V_y \times V_y) / V_x$

D) $V_o = (V_x \times V_y) / V_{ref}^2$

Answer: (B)

2. A Express the output voltage equation of divider circuit

A) $V_o = -(V_{ref}/2) \times (V_z/V_x)$

B) $V_o = -(2 \times V_{ref}) \times (V_z/V_x)$

C) $V_o = -(V_{ref}) \times (V_z/V_x)$

D) $V_o = -V_{ref}^2 \times (V_z/V_x)$

Answer: (C)

3. Which circuit can be used to take square root of a signal?

A) Divider circuit

B) Multiplier circuit

C) Squarer circuit

D) None of the mentioned

Answer: (A)

4. A trans-conductance amplifier is also called _____

A) current to voltage convertor

B) voltage to current convertor

C) resistor

D) inductor

Answer: (A)

5. Determine If the cross-sectional area of the channel in n-channel JFET increases, the drain current_____

A) is increased

B) is decreased

C) remains the same

D) decreases exponentially then increase

Answer: (A)

6. Find the voltage range at which the multiplier can be used as a squarer circuit?

A) $0 - V_{in}$

B) $V_{ref} - V_{in}$

C) $0 - V_{ref}$

D) All of the mentioned

Answer: (C)

7. A square root circuit build from multiplier is given an input voltage of 11.5v. Find its corresponding output voltage?

A) 11v

B) 15v

C) 13v

D) Cannot be determined

Answer: (D)

8. At which state the phase-locked loop tracks any change in input frequency?

A) Free running state

B) Capture state

C) Phase locked state

D) All of the mentioned

Answer: (C)

9. What is the function of low pass filter in phase-locked loop?

A) Improves low frequency noise

B) Removes high frequency noise

C) Tracks the voltage changes

D) Changes the input frequency

Answer: (B)

10. At what range the PLL can maintain the lock in the circuit?

A) Lock in range

B) Input range

C) Feedback loop range

D) None of the mentioned

Answer: (A)

11. Write the equation for time period of VCO?

A) $(2\times V_{cc}\times C_T)/i$

B) $(V_{cc}\ C_T)/(2\times i)$

C) $(V_{cc}\times C_T\times i)/2$

D) $(2\times V_{cc})/(i\times C_T)$

Answer: (B)

12. The output frequency of the VCO can be changed by changing

A) External tuning resistor

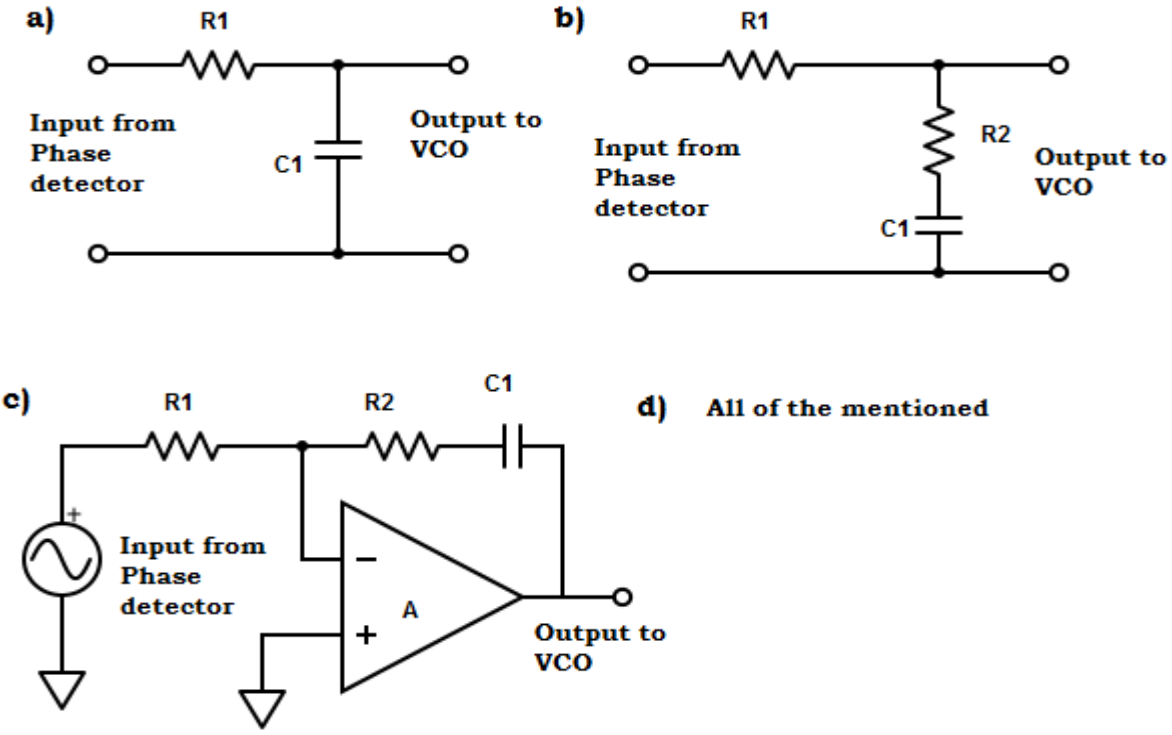
B) External tuning capacitor

C) Modulating input voltage

D) All of the mentioned

Answer: (D)

13. Which filter is used in VCO?



Answer: (D)

14. Find the equation for change in frequency of VCO?

A) $\Delta f_o = (2\times\Delta V_c)/(R_T\times C_T\times V_{cc})$

B) $\Delta f_o = \Delta V_c/(4\times R_T\times C_T\times V_{cc})$

C) $\Delta f_o = \Delta V_c/(2\times R_T\times C_T\times V_{cc})$

D) $\Delta f_o = (4\times\Delta V_c)/(R_T\times C_T\times V_{cc})$

Answer: (A)

15. For what kind of input signal, the frequency divider can be avoided frequency multiplier?

A) Triangular waveform

B) Square waveform

C) Saw tooth waveform

D) Sine waveform

Answer: (A)

16. What happens when VCO output is 90^o out of phase with respect to input signal?

A) Perfect lock

B) Attenuation

C) Shift in phase of comparator

D) Error signal is removed

Answer: (A)

17. The frequency corresponding to logic 1 state in FSK is called

A) Space frequency

B) Mark frequency

C) Both mark and space frequency

D) None of the mentioned

Answer: (B)

18. Find out the incorrect statement.

Monolithic phase detector is preferred for critical applications as it is:

1. Independent of variation in amplitude
2. Independent of variation in duty cycle of the input waveform
3. Independent of variation in response time

A) 1 & 2

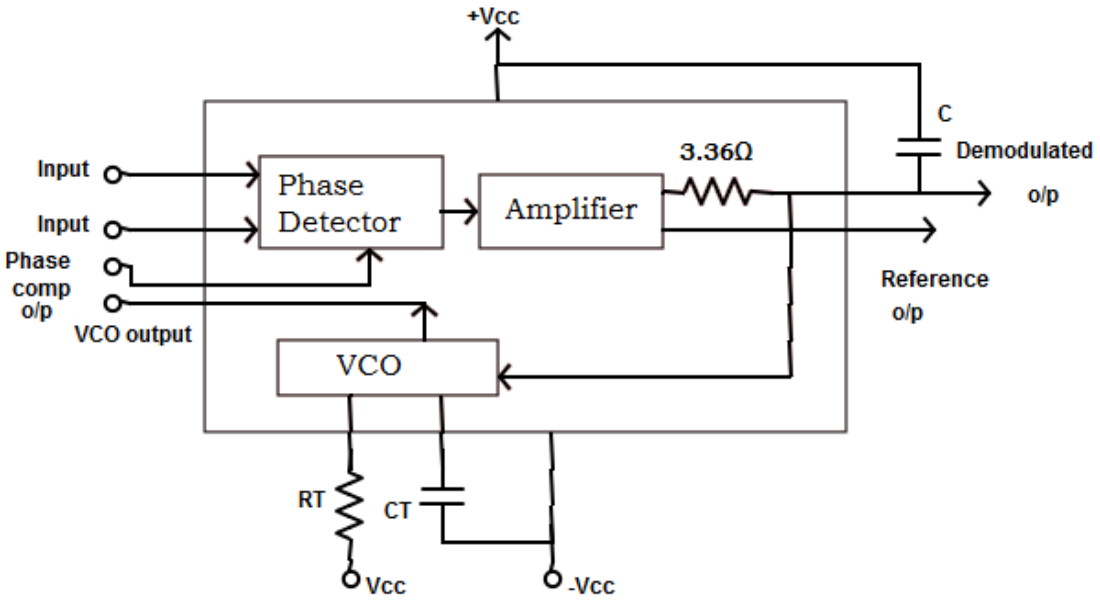
B) 1 & 3

C) 2 & 3

D) 1, 2 & 3

Answer: (A)

19. Determine the capture range of IC PLL 565 for a lock-in range of ± 1kHz.



A) $\Delta f_c = \pm 31.453Hz$

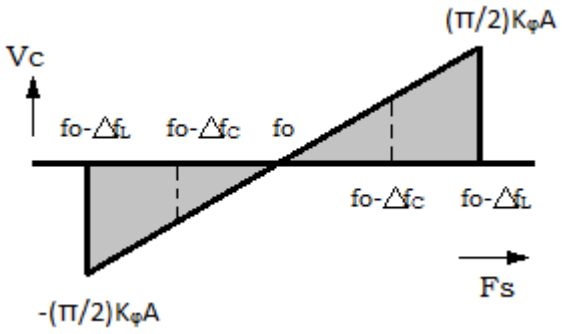
B) $\Delta f_c = \pm 66.505Hz$

C) $\Delta f_c = \pm 87.653Hz$

D) None of the mentioned

Answer: (B)

20. Find the lock-in range of monolithic Phase-Locked Loop from the given diagram.



A) $-f_o-\Delta f_L$ to $f_o-\Delta f_L$

B) $-f_o-\Delta f_L$ to $-f_o-\Delta f_C$

C) $f_o-\Delta f_L$ to $f_o-\Delta f_C$

D) $-f_o-\Delta f_C$ to $f_o-\Delta f_C$

Answer: (A)

21. At which state the phase-locked loop tracks any change in input frequency?

A) Free running state

B) Capture state

C) Phase locked state

D) All of the mentioned

Answer: (C)

22. If a process is executing in its critical section _____

A) any other process can also execute in its critical section

B) no other process can execute in its critical section

C) one more process can execute in its critical section

D) none of the mentioned

Answer: (B)

23. For proper synchronization in distributed systems _____

A) prevention from the deadlock is must

B) prevention from the starvation is must

C) prevention from the deadlock & starvation is must

D) none of the mentioned

Answer: (C)

24. The coherent modulation techniques are

A) PSK

B) FSK

C) ASK

D) All of the mentioned

Answer: (D)

25. In a The FSK signal which has a gentle shift from one frequency level to another is called as

A) Differential PSK

B) Continuous PSK

C) Differential & Continuous PSK

D) None of the mentioned

Answer: (B)